**I2S Module Description Document**

**1. Introduction**

The I2S bus provides a highly flexible digital audio communication interface for digital audio devices, specifically designed for data transmission between audio devices. The I2S bus has three main signals: bit clock (BCLK), frame clock (LRCLK), and serial data (DO/DIN). In some cases, a master clock (MCLK) may also need to be input or output to enable better synchronization between different communication devices. Additionally, the I2S bus specification defines both hardware interface specifications and audio data formats. The I2S bus data format supported by the AP80 series includes left-aligned format, right-aligned format, I2S-aligned format, and DSP format.

The master clock for the I2S module can be generated internally or supplied by an external clock. The internal clock generator can produce two types of clocks: one is an integer multiple of the sampling rate with an output of 11.2896/12.288 MHz, which AP80 refers to as NORMAL MODE; the other is a fixed 12 MHz output unaffected by the sampling rate, which AP80 refers to as USB MODE.

Additionally, the I2S module shares the same master clock source with the audio module's Audio ADC and DAC, enabling excellent synchronization among the three components.

**2. Main Features**

 Supports Master mode and Slave mode transmission;

Supports four data formats: left-aligned format, right-aligned format, I2S-aligned format, and DSP format, where the DSP format includes DSPA format and DSPB format;

Supports 16-bit data width;

Supports 9 sampling rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz;

Supports BCLK inversion;

Supports LRCLK inversion control for left-aligned format, right-aligned format, and I2S-aligned format;

 Supports PCM-SYNC format and communication with Bluetooth chips;

Supports communication with CLASS-D chips;

The I2S bus data direction is always MSB-first;

Full-duplex communication, supporting simultaneous transmission and reception;

The master clock can be output to external audio devices or provided by external audio devices;

**3. Function Description**

**3.1. Clock Description**

The master clock source for the I2S module is the same as that for the Audio ADC. For details, please refer to the “Clock Mode Block Diagram” in the Audio ADC module description. The I2S module has two clock source options: one generated by an internal generator, and the other provided by an external audio device. The internal generator supports two types of clock signal outputs: one is a clock signal at an integer multiple of the sampling rate, named NORMAL MODE in the AP80 series; the other is a fixed 12MHz clock signal, named USB MODE in the AP80 series. These two clock modes have significant differences in the I2S communication protocol.

Table 1 Relationship between LRCLK, BCLK, and MCLK in NORMAL MODE

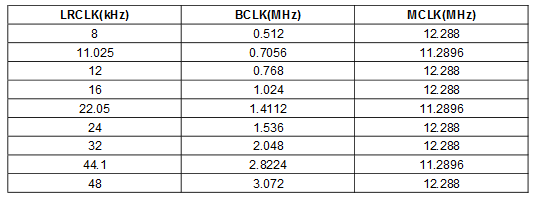
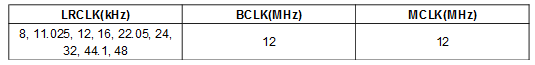


Table 2 Relationship between LRCLK, BCLK, and MCLK in USB MODE



**3.2. Operating Modes**

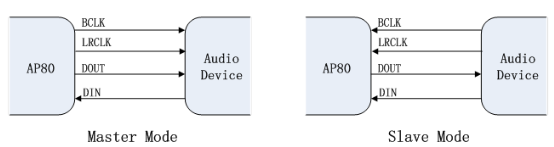


Figure 1 I2S Operating Modes

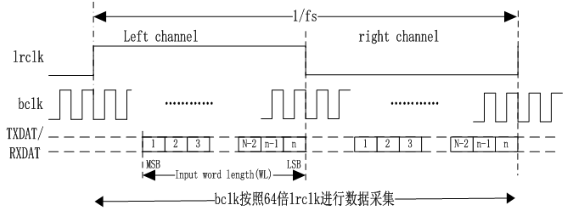
The I2S module supports Master mode and Slave mode. In Master mode, BCLK and LRCLK are generated and output by the internal clock, supporting full-duplex communication for both reception and transmission. In Slave mode, BCLK and LRCLK are no longer generated by the AP80 but are instead supplied by an external audio device.

**3.3. Data Format**

The AP80 series I2S supports four data alignment formats: right-aligned format, left-aligned format, I2S-aligned format, and DSP-aligned format, with the DSP format further divided into Mode A and Mode B. For all data formats, the most significant bit is always transmitted first, and BCLK inversion control is supported.

**3.3.1. Right-aligned format**

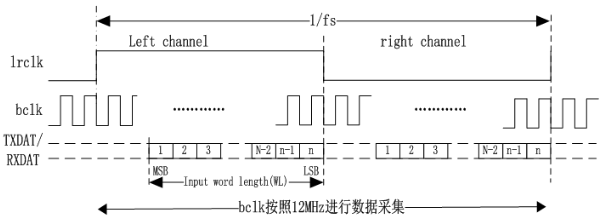
In the right-aligned format, the least significant bit (LSB) appears at the rising edge pulse of the first BCLK before the LRCLK change (i.e., the end of a frame), and the other data bits are transmitted beforehand (MSB-first). The main clock selection for USB MODE and NORMAL MODE has different BCLK values, as shown in the figure below.



Translation:

bclk按照64倍1rclk进行数据采集 = bclk collected data at 64 times 1rclk

Figure 2: Right-aligned timing diagram in NORMAL MODE



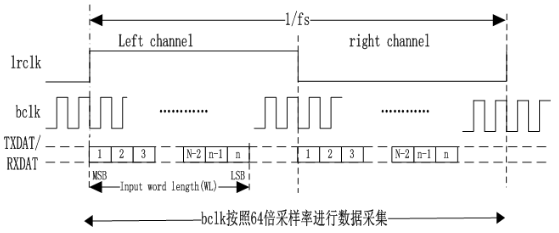
Translation:

bclk按照12MHz进行数据采集= bclk collected data at 12MHz

Figure 3: Right-aligned timing diagram in USB MODE

**3.3.2. Left-aligned format**

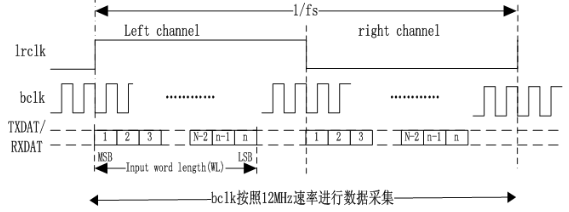
In the left-aligned format, the most significant bit (MSB) of the data always appears at the rising edge of the first BCLK pulse at the LRCLK transition (frame start). The main clock selects different clock sources, and the BCLK bit clock sampling rate varies accordingly.



Translation:

bclk按照64倍采样率进行数据采集= bclk collected data at a sampling rate of 64 times

Figure 4 Left-aligned timing diagram in NORMAL MODE



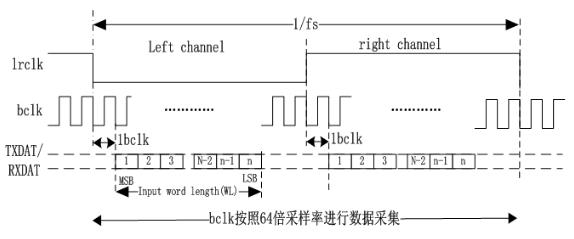
Translation:

bclk按照12MHz速率进行数据采集= bclk collected data at 12MHz

Figure 5 Left-aligned timing diagram in USB MODE

**3.3.3. I2S alignment format**

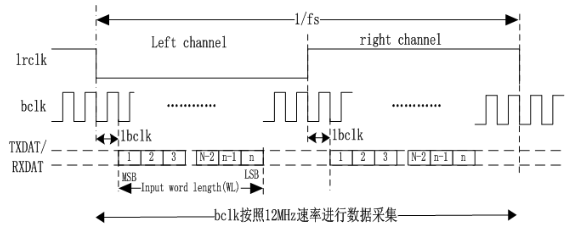
In the I2S alignment format, the most significant bit (MSB) always appears at the rising edge of the second BCLK pulse at the LRCLK transition (One frame begins). When the master clock selects different clock sources, the I2S communication protocol varies.



Translation:

bclk按照64倍采样率进行数据采集= bclk collected data at a sampling rate of 64 times

Figure 6 I2S Alignment Timing Diagram in NORMAL MODE



Translation:

bclk按照12MHz速率进行数据采集= bclk collected data at 12MHz

Figure 7 I2S Alignment Timing Diagram in USB MODE

**3.3.4. DSP Alignment Format**

In the DSP alignment format, the most significant bit (MSB) of the left-channel data may appear at the rising edge of the first BCLK pulse (Mode B) or the second BCLK pulse (Mode A) at the start of the LRCLK rising edge, with the right-channel data following immediately after the left-channel data transmission. Similarly, when the master clock selects different clock sources, the I2S communication protocol varies.

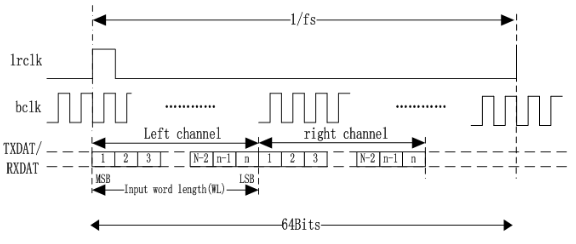


Figure 8 DSP Alignment Format in NORMAL MODE (Mode B, LRCLK not inverted)

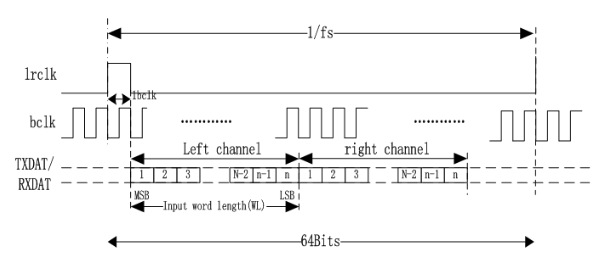
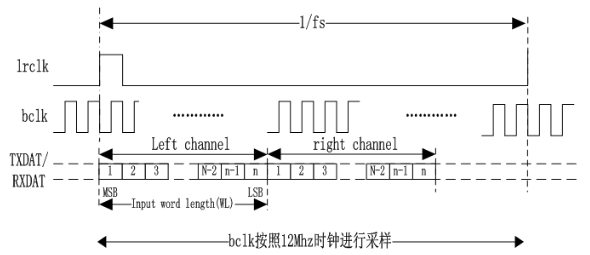


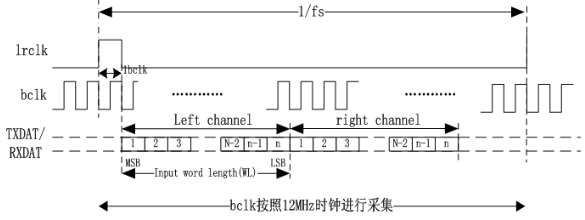
Figure 9 DSP Alignment Format in NORMAL MODE (Mode A, LRCLK inverted)



Translation:

bclk按照12MHz时钟进行采样 = bclk collected based on a 12 MHz clock

Figure 10 DSP Alignment Format in USB MODE (Mode B, LRCLK not inverted)



Translation:

bclk按照12MHz时钟进行采集 = bclk collected based on a 12 MHz clock

Figure 11 DSP Alignment Format in USB MODE (Mode A, LRCLK inverted)

In DSP alignment format Mode A, if BCLK inversion is configured, the DSP's Mode A alignment format becomes the standard PCM alignment format, supporting communication with Bluetooth chips. This format supports mono mode configuration, allowing selection between single-channel data transmission or normal data transmission.

**4. Configuration Process**

1. Standard I2S Configuration Process

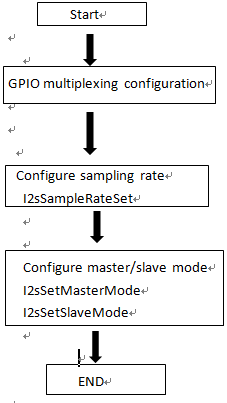
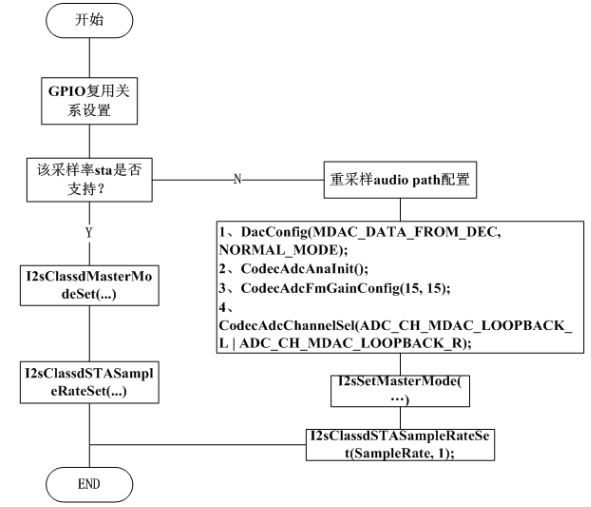


Figure 12 Standard I2S Configuration Process Diagram

2. STA-CLASSD Configuration Process



Translation：

开始= Start

GPIO复用关系设置= GPIO multiplexing relationship settings

该采样率sta是否支持？= Does this sample rate sta support?

重采样audio path配置= Resampling audio path configuration

Figure 13 STA CLASSD Configuration Process Diagram

3. Bluetooth Configuration Process

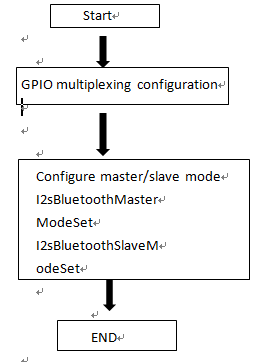


Figure 14 Bluetooth Configuration Process Diagram